AMENDMENTS TO THE SPECIFICATION:

Please insert the following before "Background of the Invention":

--This application is a divisional application of U.S. Application Serial No. 10/357,752, filed February 4, 2003, which is, in turn, a divisional application of U.S. Application Serial No. 09/741,304 filed December 19, 2000, now U.S. Patent No. 6,545,892.--

Paragraph beginning at page 2, line 14:

In the NAND circuit 100 as shown in Fig. 12, when both signals A and B are high, the serially connected nMOS transistors M_{53} and M_{54} are on (i.e., in the ON states), while the parallel-connected pMOS transistors M_{51} and M_{52} are off (i.e., in the OFF states). As a result, the electric potential of the base electrode of the BiP-Tr Q_1 becomes ground level, so that the transistor is set to the OFF state. In addition, the serially connected nMOS transistors M_{55} and M_{56} are switched on, so that the electric charges of a load (not shown) [[is]] are discharged via these transistors M_{55} and M_{56}, and the level of the output signal X_0 becomes low.

Paragraph beginning at page 7, line 10:

The ~~inventers~~ inventors of the present invention worked to reduce the occupied area of a conventional AND logic circuit (as shown in Fig. 14), and found that the size of each MOS FET as a constituent of the logic circuit can be reduced by reducing the threshold voltage value (called Vth, hereinbelow) of the FET, and accordingly, the size of the whole circuit can be reduced. That is, to reduce Vth of the MOS FET causes an increase of current flowing when a predetermined voltage is applied to the gate electrode, so that the ability to drive a transistor is improved and a smaller gate width is sufficient for providing a specific current. Therefore,

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according to the reduction of the threshold voltage value Vth of the MOS FETs in the logic circuit, the size of each transistor can be reduced and the occupied area of the whole logic circuit can be reduced.

Paragraph beginning at page 19, line 9:

In the present embodiment, the gate pattern 8 of each MOS transistor has a U-shape (i.e., folded ~~) shape~~ shape) so as to obtain a large current using a small area. Therefore, the gate width of each MOS transistor has a longitudinal direction. In addition, pMOS transistor M_{14} and nMOS transistor M_{15} form an inverter circuit 3; thus, the wiring contact indicated by reference numeral 9 functions as the output of the relevant AND logic circuit 1, and the wiring contact 9 and word lines (not shown) in each memory cell area 6 are connected. Here, 8 AND logic circuits 1, each having 5 MOS transistors arranged in the longitudinal direction as explained above, are arranged in the transverse direction, thereby forming decoder circuit 10. In addition, reference numerals 11 indicate dummy cell areas.

Paragraph bridging pages 23-24, beginning at page 23, line 17 :

As shown in Figs. 8A and 8B (enlarged view of the area surrounded by circle B in Fig. 8A), in the conventional circuit arrangement in which pMOS transistors and nMOS transistors as constituents of the circuit face each other or are arranged or aligned in the transverse direction, even if power supply lines 20 crossing memory cell areas 6 are provided, in the poly-decoder area 7, power supply lines 16 in the transverse direction can extend to the area where pMOS transistors are provided, from a relevant power supply line 15 (at the left side in Fig. 8B) in the longitudinal direction, but cannot extend to the area where nMOS transistors are provided, from a

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relevant power supply line 15 (at the right side in Fig. 8B). Therefore, power supply lines 15 which face each other via the poly decoder area 7 cannot be connected. On the other hand, each earth line 18 can extend to the area where the nMOS transistors are provided, from a relevant earth line 17 in the longitudinal direction (at the right side in Fig. 8B), but cannot extend to the area where the pMOS transistors are provided, from a relevant earth line 17 (at the left side in Fig. 8B). Therefore, earth lines 17 which face each other via the poly decoder area 7 cannot be connected. Accordingly, each memory cell area 6 has [[an]] independent wiring arrangements with respect to the power supply and earth lines, so that no wiring arrangement over a plurality of memory cell areas, that is, over the whole chip area, can be realized.

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